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REMARKS

This application has been carefully reviewed in light of the Office Action dated December 30, 2003. The drawings and specification have been amended. Claims 1, 8, 9, 11, 13, and 40-42 have been amended. Claim 10 has been canceled. Claims 32-39 were previously withdrawn. No new matter has been added. Claims 1, 4-9, 11-21, and 40-42 are now pending in this case.

The drawings are objected to for failing to show every feature of the invention specified by the claims. Specifically, the drawings are objected to for failing to show a “first cavity between the support structure and the first semiconductor die” formed under a “second cavity . . . between the first semiconductor die and the second semiconductor die.” Office Action at 2. Corrected drawings have been submitted herewith. Figure 7 has been amended to include cavity 25 between the first semiconductor die 20 and the supporting structure 10. Accordingly, withdrawal of this objection is respectfully requested.

The last paragraph beginning on page 9 of the specification, which extends to page 10, has been amended to include a description of the amendments to Figure 7. The amendments to the specification and the drawings are adequately supported. Specifically, the specification states that “the elimination of the adhesive fillet 24_b as discussed in Figure 1 covers a wide range of semiconductor configurations involving multiple dies with various sizes” Specification at 9.

Claim 41 stands rejected under 35 U.S.C. §112, first paragraph, for failing to comply with the written description requirement. This rejection is respectfully traversed.

Specifically, the Office Action states that the specification fails to disclose that a second cavity is formed on top of a first cavity. Office Action at 3. As discussed above, the drawing and specification have been amended to describe a second cavity on top of a first cavity. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claim 41 is objected to because the second occurrence of “first” should read “second.” Office Action at 2. Claim 41 has been amended to correct this informality. Therefore, withdrawal of this objection is respectfully requested.

Claims 1, 5-7, 10, 12, 40, and 42 stand rejected under 35 U.S.C. §102(b) as being anticipated by Doi et al., U.S. Patent No. 5,629,566 (“Doi”). This rejection is respectfully traversed.

The present invention relates to a semiconductor assembly. As such, amended independent claim 1 recites a “semiconductor assembly” comprising, *inter alia*, “a support structure having a top surface” and “said at least one semiconductor die being secured at its bottom surface to said top surface of said support structure solely by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die, said top surface of said support structure having at least one electrical contact area at a distance outside said perimeter of said at least one semiconductor die, said at least one semiconductor die being in electrical communication with said at least one electrical contact area.”

Amended independent claim 40 recites a “semiconductor assembly” comprising, *inter alia*, “a support structure having a top surface” and “said first semiconductor die being secured at its bottom surface to said top surface of said support structure by a compressed flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die such that there is a first cavity along at least a portion of said perimeter between said support structure and said first semiconductor die, said first cavity being filled with an encapsulating material, such that only said adhesive material and said encapsulating material are between said first semiconductor die and said support structure.” Amended independent claim 40 further recites “said top surface of said support structure having at least one electrical contact area at a distance outside said perimeter of said at least one semiconductor die, said at least one semiconductor die being in electrical communication with said at least one electrical contact area.”

Amended independent claim 42 recites a “semiconductor assembly” comprising, *inter alia*, “a support structure having a top surface” and “said at least one semiconductor die being secured at its bottom surface to said top surface of said support structure by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die, said flowable adhesive material covering an area greater than or equal to about 50% of said at least one semiconductor die’s bottom surface area, said top surface of said support structure having at least one electrical contact area at a distance outside said perimeter of said at least one semiconductor die, said at least one semiconductor die being in electrical communication with said at least one electrical contact area.”

Doi relates to a semiconductor device with a semiconductor chip connected to a circuit substrate via solder bumps by flip chip connection. Doi at Abstract. According to Doi, an encapsulant having a large Young’s modulus fills a space between the semiconductor chip and the substrate at the central portion of the semiconductor chip, whereas a second encapsulant having a small Young’s modulus fills the space between the chip and the substrate at the peripheral portion of the chip. Doi at Abstract.

Doi fails to disclose all the elements of any of independent claims 1, 40, and 41. Specifically, Doi fails to disclose “said at least one semiconductor die being secured at its bottom surface to said top surface of said support structure solely by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die,” as recited by amended independent claim 1. Also, Doi fails to disclose “a first cavity along at least a portion of said perimeter between said support structure and said first semiconductor die, said first cavity being filled with an encapsulating material, such that only said adhesive material and said encapsulating material are between said first semiconductor die and said support structure,” as recited by amended independent claim 40. Further, Doi fails to disclose “said top surface of said support structure having at least one electrical contact area at a distance outside said perimeter of said at least one semiconductor die,” as recited by amended independent claims 1, 40, and

42. In contrast, Doi discloses that a semiconductor chip is connected to a circuit substrate via solder bumps by flip chip connection, where the metallization layers on the circuit substrate contacting the bump electrodes are within the perimeter of the semiconductor die. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 1, 4-7, 10, 12-14, 40, and 42 stand rejected under 35 U.S.C. §102(b) as being anticipated by Matsumura, U.S. Patent No. 6,534,874 ("Matsumura"). This rejection is respectfully traversed.

Matsumura relates to a semiconductor device having a plurality of stacked chips. According to Matsumura, a first semiconductor chip having inner and outer electrodes is stacked below second and third chips, which each have inner electrodes. Matsumura discloses that the inner electrodes of the second and third chips each have through holes, each of which contains a plated electrode. The chips are stacked such that the inner electrodes and through holes of the second and third chips are connected to the inner electrodes of the first chip by the continuously extending plated electrodes. Matsumura also discloses that outer electrodes of the first chip are connected to a lead of a lead frame. Matsumura at col. 5, lines 11-65.

Matsumura fails to disclose all the elements of any of independent claims 1, 40, and 41. Specifically, Matsumura fails to disclose "said at least one semiconductor die being secured at its bottom surface to said top surface of said support structure solely by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die," as recited by amended independent claim 1. Also, Matsumura fails to disclose "a first cavity along at least a portion of said perimeter between said support structure and said first semiconductor die, said first cavity being filled with an encapsulating material, such that only said adhesive material and said encapsulating material are between said first semiconductor die and said support structure," as recited by amended independent claim 40. Further, Matsumura fails to disclose "said top surface of said support structure having at least one electrical contact area at a distance outside said perimeter of said at least one semiconductor die, said at least one

semiconductor die being in electrical communication with said at least one electrical contact area,” as recited by amended independent claims 1, 40, and 42. In contrast, Matsumura discloses that the first, second, and third semiconductor chips are connected to one another by inner electrodes and plated electrodes, which are within the perimeter of the chips.

Although Matsumura discloses that the first chip is joined to a die pad of a lead frame with a die bonding resin and the outer electrodes of the first chip are connected to a lead of a lead frame, Matsumura is silent about the first chip being joined to the die pad by a flowable adhesive material that does not extend past any side of the first chip. Contrarily, each of independent claims 1, 40, and 42 recite “a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die.” For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 4 and 11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Doi in view of Takiar et al., U.S. Patent No. 5,422,435 (“Takiar”). This rejection is respectfully traversed.

Claim 4 depends from amended independent claim 1 and further recites that “said support structure is at least one semiconductor die with a top and bottom surface.” Claim 11 depends from amended independent claim 1 and further recites that “said electrical communication is through a wire bond.”

Takiar relates to a circuit assembly having a semiconductor die with parallel opposing first and second surfaces with at least one electrical contact mounted on the first surface. According to Takiar, a first element with parallel opposing first and second surfaces and an electrical contact mounted on one of its surfaces is mounted by its second surface on the first surface of the semiconductor die and positioned to expose the contact on the semiconductor die. Takiar teaches that a fine wire conductor with first and second ends is connected at its first end to the semiconductor die contact and at its second end to the first element contact. Takiar at col. 3, lines 28-41.

In order to establish a prima facie case of obviousness, there must be some motivation in the prior art to modify or combine the cited references. MPEP § 2142. The Office Action states that it would have been obvious to modify Doi by using the semiconductor die for the support structure and a wire bond for electrical communication as taught by Takiar to provide an easy and low cost stacked semiconductor package. Office Action at 9.

The Applicant respectfully submits that there is no motivation to modify Doi with the teachings of Takiar, and that, in fact, the references teach away from the proposed modification. Specifically, Doi teaches a semiconductor device with a semiconductor chip connected to a circuit substrate via solder bumps by flip chip connection. Doi at Abstract. Doi states that “in order to assemble the semiconductor element with the circuit substrate . . . mounting the semiconductor chip directly to the circuit substrate to connect them to the metallization pattern by wire bonding or TAB (Tape Automated Bonding), have been used. However, the method of providing outer leads on the chip and mounting them on the circuit substrate [is] a serious impediment to the development of high density assembly technology” Doi at col. 1, lines 12-30. Moreover, Takiar states that “‘flip chip’, involves the use of a large number of solder bumps on a die surface which allow it to be bonded face down. . . . [D]isadvantages include requirements for precise alignment, difficulties in cleaning and inspection, uniform solder joint height for all connection to be made and a substrate with low coefficient of thermal expansion Furthermore . . . after the dice are stacked, no additional interconnections can be made.” Takiar at col. 2, line 64-col. 3, line 10. It is clear that Doi and Takiar teach distinct techniques. Therefore, one of ordinary skill in the art would not have been motivated to modify the teachings of Doi with the teachings of Takiar to provide wire bonds.

To modify Doi with the teachings of Takiar would impermissibly require a substantial reconstruction and redesign of the elements of Doi and change the principle under which Doi was designed to operate. MPEP § 2143.01. As noted above, Doi fails to disclose “said at least one semiconductor die being secured at its bottom surface to said

top surface of said support structure solely by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die” and “said top surface of said support structure having at least one electrical contact area at a distance outside said perimeter of said at least one semiconductor die,” as recited by amended independent claims 1. Instead, Doi teaches that a semiconductor chip is connected to a circuit substrate via solder bumps by flip chip connection, where the contact area on the circuit substrate is within the perimeter of the semiconductor die, which is essential to Doi. Therefore, Doi, even when considered with Takiar, does not render claims 4 or 11 obvious. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 8 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Doi in view of McMahon, U.S. Patent No. 6,075,712 (“McMahon”). This rejection is respectfully traversed.

Amended claim 8 depends from amended independent claim 1 and further recites that “a distance between said electrical contact area and said perimeter of said at least one semiconductor die is less than or equal to about 428 microns.” Amended claim 9 depends from amended independent claim 1 and further recites that “a distance between said electrical contact area and said perimeter of said at least one semiconductor die is less than or equal to about 200 microns.”

McMahon relates to “a flip-chip having bond pads on the backside of the chip that are electrically coupled to active devices in the chip.” McMahon at col. 1, lines 7-10. McMahon teaches an assembly including a chip that is coupled to a package substrate through a conductor region on a front surface of the chip. The conductor region has contact pads which are coupled to the package substrate by solder bonds. McMahon at col. 4, lines 35-38. On the backside of the chip, McMahon discloses that there are contact pads connected to wires, which in turn are connected to bond pads on the package substrate. McMahon at col. 3, lines 15-36.

Doi, even when considered together with McMahon, fails to teach or suggest all the limitations of amended independent claim 1. As noted above, Doi fails to teach or suggest “said at least one semiconductor die being secured at its bottom surface to said top surface of said support structure solely by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die,” as recited by amended independent claim 1. McMahon teaches that the chip is connected to the package substrate by solder bonds (McMahon at col. 4, lines 35-38) and is silent about any flowable adhesive, much less “said at least one semiconductor die being secured at its bottom surface to said top surface of said support structure solely by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die,” as recited by amended independent claim 1. Thus, Doi, even when considered with McMahon, fails to teach or suggest all the limitations of amended independent claim 1.

Also, the Office Action states that McMahon shows in Fig. 5A an electrical contact area 254 extending under the perimeter of a semiconductor die, and therefore McMahon teaches that a distance between the bond pad and the perimeter of a chip is less than or equal to about 200 microns. Office Action at 9. Applicant agrees that if the bond pad is directly below the chip and within the perimeter of the chip, there is a distance of less than 200 microns between the bond pad and the perimeter of the chip. However, Fig. 5A does not appear to show this. Furthermore, amended independent claim 1 recites “said top surface of said support structure having at least one electrical contact area at a distance outside said perimeter of said at least one semiconductor die.” Accordingly, even if McMahon’s Fig. 5A shows the bond pad within the perimeter of the chip, such a showing fails to teach or suggest this limitation. Moreover, Applicant submits that McMahon is silent about the distance of the bond pad from the perimeter of the chip where McMahon shows the bond pad outside the chip perimeter. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 13 and 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Doi in view of Fukui et al., U.S. Patent No. 6,100,594 ("Fukui"). This rejection is respectfully traversed.

Claim 13 depends from amended independent claim 1 and further recites that "an encapsulating material for encapsulating said die, electrical communication, and at least a portion of said support structure." Claim 14 depends from amended independent claim 1 and further recites that "said encapsulating material fills in at least some portion of a space between said bottom surface of said die and said top surface of said support structure."

Fukui relates to a semiconductor device and method of forming the same. Fukui teaches producing a semiconductor chip by affixing a thermo compression sheet to the back surface of a wafer, which has a circuit formed on its front side. The first chip is mounted to a printed circuit board. According to Fukui, a second semiconductor chip produced in the same manner as the first chip is mounted on the first chip. The first and second chips are wire bonded to the circuit board. The first and second chips and the wires are covered by a sealing resin. Fukui at Abstract.

Doi, even when considered in combination with Fukui, fails to teach or suggest all the limitations of amended independent claim 1. As discussed above, Doi fails to teach or suggest "said at least one semiconductor die being secured at its bottom surface to said top surface of said support structure solely by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die," as recited by amended independent claim 1. Instead, the crux of Doi is a semiconductor chip is connected to a circuit substrate via solder bumps by flip chip connection. Fukui also fails to teach or suggest "a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die," as recited by amended independent claim 1. Instead, Fukui teaches that a thermo compression sheet is used to mount the first chip to the insulating layer of the printed circuit board. Fukui at Abstract.

Further, the Applicant respectfully submits that there is no motivation to modify Doi with the teachings of Fukui, and that, in fact, the references teach away from the proposed modification. As noted above, Doi states that “in order to assemble the semiconductor element with the circuit substrate . . . mounting the semiconductor chip directly to the circuit substrate to connect them to the metallization pattern by wire bonding or TAB (Tape Automated Bonding), have been used. However, the method of providing outer leads on the chip and mounting them on the circuit substrate [is] a serious impediment to the development of high density assembly technology” Doi at col. 1, lines 12-30. Therefore, one of ordinary skill in the art would not have been motivated to modify the teachings of Doi with to teachings of Fukui to achieve the claimed invention. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 8, 9, 15-17, and 19-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Matsumura in view of McMahon. This rejection is respectfully traversed.

Independent claim 15 recites a “semiconductor assembly” comprising, *inter alia*, a first semiconductor die having a top and a bottom surface” and “a second semiconductor die having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die, said second die being secured at its bottom surface to said top surface of said first semiconductor die by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said second semiconductor die.” Independent claim 15 further recites that “said top surface of said first semiconductor die has at least one electrical contact area positioned at a location exterior to said perimeter of said second semiconductor die” and “a distance between said electrical contact area and said perimeter of said second semiconductor die is less than or equal to about 428 microns.”

Matsumura, even when considered in combination with McMahon, fails to teach or suggest all limitations of amended independent claim 1 and independent claim 15. As discussed above, Matsumura fails to teach or suggest “said at least one semiconductor die

being secured at its bottom surface to said top surface of said support structure solely by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die,” as recited by amended independent claim 1. Likewise, as discussed above in connection with the 35 U.S.C. § 103 rejection of claims 8 and 9, McMahon fails to teach or suggest “said at least one semiconductor die being secured at its bottom surface to said top surface of said support structure solely by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die,” as recited by amended independent claim 1. Thus, Matsumura, even when considered with McMahon, fails to teach or suggest all the limitations of amended independent claim 1 from which claims 8 and 9 depend.

Further, and as noted by the Office Action, Matsumura fails to teach or suggest “said top surface of said first semiconductor die has at least one electrical contact area positioned at a location exterior to said perimeter of said second semiconductor die” and “a distance between said electrical contact area and said perimeter of said second semiconductor die is less than or equal to about 428 microns,” as recited by independent claim 15. Emphasis added; see Office Action at 11. As discussed above in connection with the 35 U.S.C. § 103 rejection of claims 8 and 9, even if McMahon’s Fig. 5A shows the bond pad within the perimeter of the chip, such a showing fails to teach or suggest these limitations. As also noted above, McMahon is silent about the distance of the bond pad from the perimeter of the chip where McMahon shows the bond pad outside the chip perimeter. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 11 and 41 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Matsumura in view of Takiar. This rejection is respectfully traversed.

Matsumura, even when considered in combination with Takiar, does not render the subject matter of claims 11 or 41 obvious. One of ordinary skill in the art would not have been motivated to modify the teachings of Matsumura with the teachings of Takiar to achieve the invention as claimed by amended independent claims 1 and 40, from which claims 11 and 41 respectively depend.

As noted above in connection with the 35 U.S.C. §102 rejection of claims 1, 4-7, 10, 12-14, 40, and 42, Matsumura fails to disclose “a first cavity along at least a portion of said perimeter between said support structure and said first semiconductor die, said first cavity being filled with an encapsulating material, such that only said adhesive material and said encapsulating material are between said first semiconductor die and said support structure,” as recited by amended independent claim 40. Additionally, Matsumura fails to disclose “said top surface of said support structure having at least one electrical contact area at a distance outside said perimeter of said at least one semiconductor die, said at least one semiconductor die being in electrical communication with said at least one electrical contact area,” as recited by amended independent claims 1 and 40.

Instead, Matsumura teaches that the inner electrodes of the second and third chips each have through holes containing a plated electrode, and that the chips are stacked such that the inner electrodes and through holes of the second and third chips are connected to the inner electrodes of the first chip by the continuously extending plated electrodes. In this manner, Matsumura allows connections to the front and backsides of chips stacked on the circuit substrate. The inner electrodes, which are within the perimeter of the stacked chips, are essential to Matsumura. To modify Matsumura with the teachings of Takiar would impermissibly change the principle under which Matsumura was designed to operate. MPEP § 2143.01. Therefore, Matsumura, even when considered with Takiar, does not render claims 11 or 41 obvious. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claim 18 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Matsumura in view of McMahon and in further view of Crowley et al., U.S. Patent No. 6,459,147 (“Crowley”). This rejection is respectfully traversed.

Crowley relates to a method and apparatus for electrically connecting a semiconductor die to a substrate, such as a lead frame. According to Crowley the die is mounted with a conductive strap, such that the connection is more resistant to stress induced by temperature changes. Crowley at col. 1, line 66 –col. 2, line 4.

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As noted above, Matsumura, even when considered in combination with McMahon, fails to teach or suggest all the limitations of independent claim 15. Crowley fails to supplement the deficiencies of Matsumura and McMahon. Specifically, like Matsumura and McMahon, Crowley fails to teach or suggest "said top surface of said first semiconductor die has at least one electrical contact area positioned at a location exterior to said perimeter of said second semiconductor die" and "a distance between said electrical contact area and said perimeter of said second semiconductor die is less than or equal to about 428 microns," as recited by independent claim 15 from which claim 18 depends. For at least these reasons, withdrawal of this rejection is respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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